2nd EUJAPAN
DIGITAL WEEK 2026

23 March – 30 March 2026
Tokyo, Japan

The EU-Japan Digital Week is organised as part of the EU-Japan Digital Partnership

Semiconductor Workshop: “Japan-EU Cooperation on Advanced Computing, Advanced Functionalities and Semiconductor Value Chain” (DAY 2)

- **Date:** Wednesday, 25 March
- **Time:** 08:45-17:30 Japan Standard Time (JST)
- **Location:** **Location:** HASEKO-KUMA HALL: https://haseko-kuma.t.u-tokyo.ac.jp/access/ 7-3-1 Hongo, Bunkyo-ku, Tokyo, Japan. The University of Tokyo
- **Organiser:** Dr. Francis Balestra, SiNANO Institute/CNRS, INPACE, France
- **Co-organiser:** Prof. Ken Uchida, The University of Tokyo, Japan
- **Summary:** The workshop will focus on key areas of the INPACE Cluster dedicated to “Enabling technologies - Chips for the future” and is aligned with the topics defined in the Digital Partnerships between EU and Japan. The presentations and discussions will cover the many semiconductor challenges (complex value chain, computing and storage needs, novel functionalities for electronic systems, circuit and system integration, energy & material needs, reliability) and possible technological solutions, especially: reductions of energy and material consumption for sustainable electronic systems, advanced logic devices and materials, integration of novel functionalities for future electronic systems (smart sensing, energy harvesting for autonomous system, cryoelectronics for quantum engineering), heterogeneous 3D integration and packaging for high performance, low power, low latency, miniaturisation, integration of new functionalities and lower cost of electronic systems, and possible cooperation on gaps in the semiconductor value chain.

Agenda

8:45 - 10:00 Session 1 – Heterogeneous Integration and Advanced Packaging

- **Applied Research in 3d Heterogeneous Integration and Advanced Packaging of Next Generation Semiconductor Products**
  Patrick Bressler, Fraunhofer, Germany
- **Interconnects for AI in the 3D Chiplet Era: Japan's Ecosystem View**
  Fumihiro Inoue, Yokohama National University, Japan
- Mitsumasa Koyanagi, Tohoku University, Japan

10:00 - 10:15 Coffee Break

10:15 - 11:25 Session 2 – New Channel Materials

- Kaoru Toko, University of Tsukuba, Japan
- **2D channel materials**
  Burkay Uzlu, AMO GmbH, Germany
- Kazuhito Tsukagoshi, NIMS, Japan

11:25- 12:15 Session 3 – Semiconductor technology, value chain and projects for possible international cooperation

- **Semiconductor technologies, value chain and projects for possible international cooperation**
  Dr. Francis Balestra, CNRS, France
- **Crypto Hardware Accelerator Design and Rapid Chips Design & Fabrication Platform**
  Makoto Ikeda, University of Tokyo, Japan

12:15 - 13:30 Lunch Break

13:30 - 14:20 Session 4 – Power Devices

- **Gallium oxide power device technologies**
  Masataka Higashiwaki, Osaka Metropolitan University, Japan
- **Widebandgap and ultrawide-bandgap power devices**

14:20 - 15:10 Session 5 – Memory Technologies

- **DFT and Quantum Transport Simulations of 2D Material-Based Resistive Memories**
  Alessandro Cresti, CNRS, France
- **Low Power Nonvolatile NBFPGA for Space and Cryogenic Applications**
  Munehiro Tada, Keio University, Japan

15:10 – 15:25 Coffee Break

15:25- 16:15 Session 6 - Optoelectronics

- **Semiconductor-based photonics and optoelectronics**
  Abdul Rahim, PhotonDelta, Belgium

- **Photonic Integrated Circuits with Heterogeneous Material Integration and Photonics**
  Nobuhiko Nishiyama, Institute of Science Tokyo, Japan

16:15 - 16:40 Session 7 – International Cooperation
- **Japan-EU JASMINE Chips Project**
  Mircea Modreanu, Tyndall National Institute, Ireland

16:40 - 17:05 Plenary
- Atsuyoshi Koike, Rapidus, Japan

17:05 - 17:30 Closing Remarks
- Ken Uchida, University of Tokyo, Japan